CLAIMS

1. A translator unit for translating a packet formatted according to a first protocol into a packet according to a second protocol, the translator unit comprising:

an input memory;

at least one information source;

an output memory;

a connection circuit, coupled to the input memory, the information source and the output memory, to selectively connect the input memory and the information source to the output memory; and

a microcoded control unit coupled to the connection circuit.

2. The translator unit of claim 1, wherein the information source is selected from the group consisting of a register, a FIFO memory, a random access memory and an opcode memory storing data as operands of microcoded instructions.

3. The translator unit of claim 1, wherein the microcoded control unit includes a pipeline unit.

4. The translator unit of claim 1, wherein the microcoded control unit includes two pipeline units.

5. The translator unit of claim 4, wherein:

the output memory includes at least two inputs to simultaneously write at least two bytes of data into the output memory; and

the connection circuit includes means for aligning the two bytes of data to be simultaneously written into the output memory.

6. The translator unit of claim 1, wherein the microcoded control unit includes four pipeline units.

7. The translator unit of claim 6, wherein:

the output memory includes at least four inputs to simultaneously write at least four bytes of data into the output memory; and

the connection circuit includes means for aligning the four bytes of data to be simultaneously written into the output memory.

8. The translator unit of claim 1, further comprising a direct memory access controller coupled to the input memory and the output memory.

9. The translator unit of claim 1, wherein the microcoded control unit includes an opcode memory programmed to perform multiple different protocol translations.

10. A pipelined control unit for reading data, comprising:

a first memory having a first read latency;

a second memory having a second read latency, longer than the first read latency;

a pipeline unit having a first stage and a second stage;

a circuit, coupled to the pipeline unit, the first memory and the second memory, to initiate read cycles from the first memory based on a first instruction in the second stage of the pipeline, and to initiate read cycles from the second memory based on a second instruction in the first stage of the pipeline.

11. The pipelined control unit of claim 10, further comprising a microcontroller coupled to the circuit.

12. A method of translating an original packet from a first protocol to a second protocol, comprising steps of:

loading a first memory with a plurality of sets of microcode instructions, each set being designed to perform a different network communication protocol translation;

receiving the original packet;

selecting a one of the sets of microcode instructions, based on the identity of the first protocol and the identity of the second protocol; and

translating the original packet into a translated packet by executing the selected set of microcode instructions.

13. The method of claim 12, wherein the translating step includes a step of feeding the microcode instructions through a pipeline.

14. A method of translating an original packet into a translated packet, comprising steps of:

loading an instruction memory with a set of instructions;

loading the original packet into an input memory, the input memory having a first read latency;

providing an information source;

providing an output memory to store the translated packet;

sequentially, selectively connecting the input memory and the information source to the output memory, based on the instructions.

15. The method of claim 14, wherein the loading step comprises a step of loading microcoded instructions.

16. The method of claim 14, wherein the connecting step comprises a step of feeding the instructions through a pipeline unit.

17. The method of claim 16, wherein:

the pipeline unit has a plurality of stages;

the set of instructions includes a first instruction to read information from the input memory and write the information to the output memory, and a second instruction to read information from the information source and write the information to the output memory; and

the connecting step comprises steps of

initiating reads from the input memory when the first instruction is at a one of the pipeline stages selected based on a read latency for the input memory; and

initiating reads from the information source when the second instruction is at a one of the pipeline stages selected based on the second read latency.

18. The method of claim 17, wherein the connecting step comprises a step of connecting the input memory to the output memory when the first instruction reaches a one of the pipeline stages after the pipeline stage where the first instruction initiated reading of the input memory.

19. The method of claim 14, further comprising a step of transferring a payload portion of the original packet from the input memory to the output memory using a direct memory access controller.

20. The method of claim 14, wherein:

the connecting step includes a step of connecting a plurality of data channels to the output memory.

21. The method of claim 20, further comprising a step of storing data in an alignment storage unit to align data on the data channels to be simultaneously written to the output memory.